What is claimed is:

1. A memory card comprising:

an electrically rewritable non-volatile memory;

a data processor having a function of executing instructions and managing the allocation of file data in said non-volatile memory;

an interface control circuit, having a function of establishing external interface, controlling the execution of instructions by said data processor in response to external commands and controlling access to said non-volatile memory; and

a buffer memory temporarily storing said file data, wherein said interface control circuit includes command control circuit decoding a first command supplied from an outside and instructing said data processor to fetch an instruction from said buffer memory and to operate.

2. A memory card according to Claim 1, wherein said command control circuit requests said data processor an interrupt and notifies it of a first cause of interrupt by decoding said first command.

3. A memory card according to Claim 2, wherein said data processor includes a central processing unit capable of responding to an interrupt by transferring the process to an instruction address

indicated by a vector retrieved from a vector table according to a cause of interrupt and a ROM to be accessed by said central processing unit;

said ROM includes said vector table and a program area; and

said vector table includes a first vector associated with said first cause of interrupt.

4. A memory card according to Claim 3, wherein

said command control circuit further requests said data processor an interrupt and notifies it of a second cause of interrupt by decoding a second command supplied from the outside;

the vector table in said ROM further includes a second vector that responds to said second cause of interrupt;

the program area of said ROM further includes a transfer control program for storing said program supplied from the outside in said buffer memory starting from a first address thereof;

said second vector is information indicating the leading address of said transfer control program; and

said first address is an address that coincides with the address indicated by said first vector.

5. A memory card according to Claim 3, wherein

said command control circuit further requests

said data processor an interrupt and notifies it of a third cause of interrupt by decoding a third command supplied from the outside;

the vector table in said ROM further includes a third vector that responds to said third cause of interrupt;

the program area of said ROM further includes a transfer control program for storing the program supplied from said non-volatile memory in said buffer memory starting from a first address thereof;

said third vector is information indicating the leading address of said transfer control program; and

said first address is an address that coincides with the address indicated by said first vector.

6. A memory card according to any one of Claims 1 through 5 formed on a single semiconductor chip.